REMARKS

Claim 12 is amended in response to the Examiner's objection to that claim. Claims 1 and 4 are amended in a further effort to define novel and unobvious subject matter over the art of record. Claims 1-12 remain, with no claim previously allowed.

Claims 1 and 9 were rejected as anticipated by *Hill* (US 6,028,348). The Applicant respectfully traverses this rejection, as possibly applied to the amended claims.

The rejection of Claim 1 as lacking novelty is based on the assumption that the metallization layer, which comprises the metal contact to the collector of the active component (e.g., Fig. 5b of *Hill*) is also a wiring level of the integrated circuit described in that document. However, as described in column 4, lines 25-27 of *Hill*, the metallization layer deposited via evaporation and liftoff only defines *collector* contacts. Similarly, *Hill* describes (column 4, lines 11-15) the formation of metallization layers defining base and emitter contacts.

In contrast with *Hill*, in the integrated circuit according to the present invention the metallization layer comprising a metal contact of the at least one active component is formed to be a wiring level, i.e., a conductive layer, which forms the wiring for connecting different components of the integrated circuit. This has the advantage that the integrated circuit can be produced more cost effectively and with a higher degree of integration, because one further metallization layer may be rendered dispensable as its function is taken over by the metallization layer comprising the metal contact of the at least one active component.

In order to clarify that aspect of the present invention and to further define over *Hill*, Claim 1 is amended to require that the lower one of the wiring levels "connects the

at least one active component with at least one passive component". This additional feature is described in the specification on page 4, lines 9-12, where the "passive component" is a resistor.

Hill does not disclose the integrated circuit arrangement now defined by Claim 1, and so that claim, as well as Claim 9, is novel over *Hill*.

Claim 3 is rejected as being unpatentable over *Hill*. The Applicant respectfully traverses that rejection, for the reasons discussed above and for the following reasons.

The rejection argues that *Hill* has a resistor formed in a wiring level by means of an interruption in the metallization layer. However, column 7, lines 58-61 of *Hill* (cited by the Examiner in support for his argument) only discloses a method of defining a location in the integrated circuit, in which a common thin film resistor is to be placed. Therefore, in order to obtain an electric resistor according to the teaching of *Hill*, one needs to add additional resistive material during the manufacturing process of the integrated circuit. Such resistive material is <u>not</u> required, however, when producing an electric resistor according to the embodiment of Claim 3 in the present application. Instead, the resistive properties of the semiconducting sub-collector layer are utilized. Because the semiconducting sub-collector layer underneath the metallization layer (which is formed to be a wiring level) remains in place, an electric resistor may be formed by a simple interruption in the metallization layer without adding any further resistive material.

In order to support the foregoing position of the Applicant and to overcome the rejection of the embodiment according to Claim 3, the Applicant has amended that claim to specify that --no additional resistive material is placed in the interruption of the

metallization layer--. This requirement of Claim 3 is, as mentioned above, contrary to the teaching of *Hill* at column 7, lines 58-61. Accordingly, one of ordinary skill would not have found, in that reference, any teaching for the integrated circuit arrangement as now defined in Claim 3, and so that claim is patentable over *Hill*.

Claims 2, 4-8 and 12 are rejected as unpatentable over *Hill* in view of *Ko* (US 2001/0053840). *Ko* is cited as teaching a small dielectric consistent below three. However, nothing in that reference nor in the primary reference *Hill* teaches or suggests an integrated circuit including the limitations of parent Claim 1, namely, that a particular wiring level connects the at least one active component with at least one passive component. Failing that teaching in the art applied to Claims 2, 4-8, and 12, those claims define unobvious and therefore patentable subject matter over that art.

Claim 10 is rejected as unpatentable over *Hill* in view of *Ko*, further in view of *Baba* (US 6,853,054). *Baba* is cited as disclosing a microstrip conductor formed by means of various wiring levels in a semiconductor device. However, neither that reference, nor *Hill* and *Ko*, disclose or suggest the novel combination of structural elements now recited in parent Claim 1. For that reason, Claim 10 is patentable over the applied art.

Claim 11 is rejected as unpatentable over *Hill* in view of *Shimamoto* (US 6,683,260). *Shimamoto* is cited as disclosing a waveguide in a multilayer wiring board. However, that reference and the other two references fail to disclose or teach an integrated circuit arrangement having the novel combination of elements as comprised in parent Claim 4, discussed above. Accordingly, the integrated circuit arrangement of Claim 11 would not have been obvious to one of ordinary skill in view of the applied art.

The foregoing is submitted as a complete response to the Office action identified above. The Applicant respectfully submits that this application is in condition for allowance and solicits a notice to that effect.

Respectfully submitted,

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